LONGITUDINAL FEEDBACK SYSTEM SOFTWARE DEVELOPMENT IN TLS

C. H. Kuo, W. K. Lau, M. S. Yeh, C. J. Wang, K. T. Hsu
Synchrotron Radiation Research Center
No. 1 R&D Road VI, Hsinchu Science-Based Industrial Park, Hsinchu 30077, Taiwan, R.O.C

Abstract

A digital signal processor (DSP) based longitudinal multi-bunch feedback system is being developed in TLS Taiwan Light Source (TLS)[1,2]. The feedback system consists of a DSP array to execute a feedback algorithm and to provide raw data for diagnostic purposes. It also consists of a simulation tool to develop and adjust parameter for the system. In order to develop, commission, and operate this system efficiently, an integrated software environment has been developed. A commercial off-the-shelf product solution was selected for the DSP environment to save development time. This network based DSP development environment provides a convenient way to code debug, beam test, and execute control rules. System simulation tools on a console computer are integrated with clients to operate this feedback system. The preliminary test results and development status will be discussed in this report.

1 INTRODUCTION

The software structure of longitudinal multi-bunch feedback system (LFB) consists of a DSP array to execute a feedback algorithm and to provide raw data for beam diagnostic purposes. In order to develop, commission, and operate this system efficiently, an integrated software environment has been developed. In this environment, the major software components include, (1) a feedback control algorithm on DSP, (2) the DSP development environment on personal computer (PC), (3) diagnostics toolkits on PC, and embedded computer, (4) and an operator interface on PC, and workstation. The feedback control loop is combined with digital filter and controller. The DSP development environment includes a code composer running on a PC as well as a remote Ethernet based JTAG emulator for program debugging. The system will use diagnostic toolkits to acquire and analyze data. The associated hardware and software are commercial products that may help reduce the system development time.

2 SOFTWARE DIAGRAM

2.1 Network Server

The network server handles all service tasks. It supports feedback loop control, filter update, and data acquisition. The hardware for this server is a VME bus/master interface card. It consists of a PowerPC 604e microprocessor, 32 megabytes on-board memory, RS-232, PMC sites, and Ethernet ports.

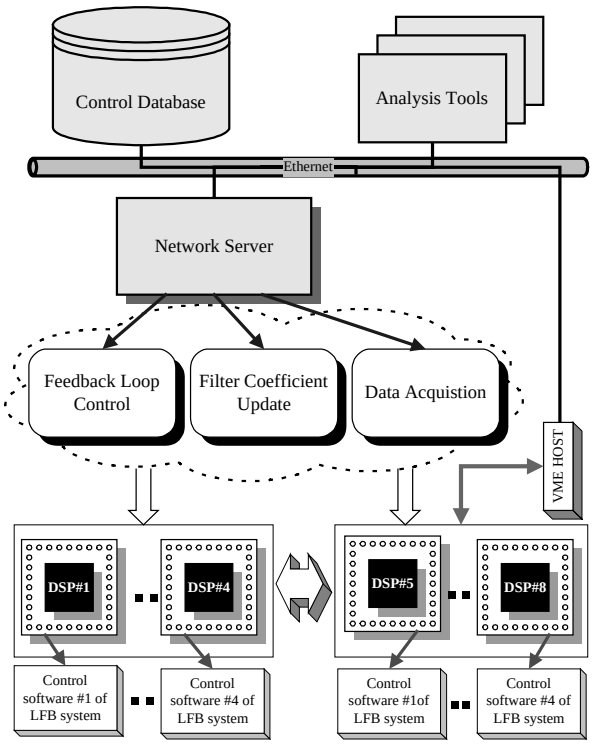

Figure 1. LFB Software Diagram.

There are a few tasks that may be developed in the VME bus host. This is a DSP debugger and development environment. But this isn't enough for analysis and access request [3].

2.2 Feedback Loop Control

The feedback loop control task manages the operation of the LFB system. The control database sends control signal to the network server. The server generates relative events to coordinate the operation of various software components.

2.3 Filter Coefficient Update

The filter coefficients of longitudinal feedback loop must be easily updated in order to respond to various conditions. The filter coefficients are stored in a file. This

file is transferred from disk to the network server by network file server (NFS). All experimental data are also saved to this disk.

2.4 Data acquisition

The data acquisition is to access slave interface card of VME bus from Power PC 604e main board that is master of VME bus. The DSP board is configured as a slave interface card on the VME bus. The dual port memory of the DSP is global and shared on the VME bus. The diagnostic data is saved to this area periodically. The master card isn't deterministic to access DSP memory and doesn't influence feedback loop of LFB.

3 DEBUG ENVIRNOMENT

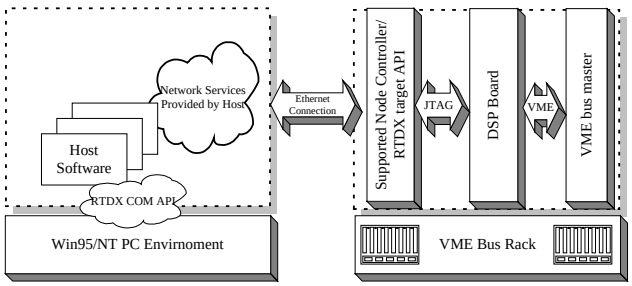

Figure 2. The schematic diagram of debugger and development environment.

The debugger and development environment of the VME host provides a simple, interrupt-driven, inter-device communication protocol for distributed DSP applications. This protocol is based on high-level geographic addressing, in which each device is referred to by a user assigned name rather than as a range of addresses. The hardware involved in these distributed applications utilize various interconnect schemes, such as shared memory on the VME bus or MIX bus Ethernet, etc. The debugging tool provides a variety of capabilities. These include, starting, stopping or resetting the DSP, loading code or data into the DSP, examining the registers or memory of DSP, and setting hardware instruction or data-dependent breakpoints. Also included are a variety of counting capabilities including cycle-accurate profiling and real-time data exchange (RTDX) between the host and the DSP. The schematic diagram of system is shown in figure 2.

RTDX provides continuous visibility into the way the DSP applications operate in the real world. RTDX allows system developers to transfer data between a host computer and DSP devices without stopping their target application. The system is paused for a short time while data is transferred. Although this environment isn't enough for the feedback loop of the system, it can support easy program debugging and development. The data of RTDX can be analyzed and visualized on the host using any OLE automation client. This shortens development time by giving designers a realistic representation of the way their systems actually operate.

4 I/O INTERFACE

There is another interface between the digital parallel input and the digital parallel output for analog to digital and digital to analog devices, except that the debugger and development of VME host and data acquisition [4]. This interface is compatible with a Texas Instruments TMS320C4x Communication port (Comm port). The Comm port interface card is a VIM-2 mezzanine module, which mounts on two adjacent mezzanine connectors on the DSP boards.

The Comm ports are byte-serial communication links capable of delivering data at sustained rate of 16.6 MB/sec using standard flat ribbon cable. Front panel multi-pin connectors allow easy cabling and reconfiguration of the data path. The Comm port module may be attached to a DSP board to provide eight split Comm ports, while occupying only one VME bus slot.

A Comm port interface engine provides timing, handshaking and data packing for both input and output data transfers. The interface engine connects to the 32-bit BI-FIFO and can be individually configured for either input or output operation. The system block is shown in figure 3.

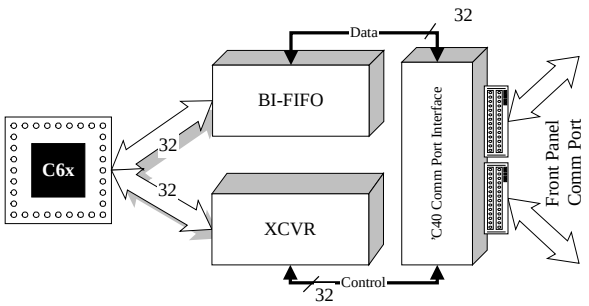

Figure 3. The system block of Comm port interface.

5 CONCLUSION

The preliminary test has suppressed longitudinal oscillation successfully. Analog input of the LFB electronics has been connected to Comm port of the DSP modules. This testing is a single bunch longitudinal oscillation that is suppressed by the feedback loop and kicker. The synchrotron sideband is suppressed when feedback is turned on. The DSP board is going to be upgraded to new DSP boards that consist of four TMS320C6201. CPU power is enough to perform the infinite impulse response filtering (IIR) for 25 bunches per processor [6]. Parts of the LFB electronics are still in the implementation stage. The analog input has been tested in the single bunch feedback loop. The output

electronics are been testing now. The diagnostic software for the longitudinal feedback system has been developed in DSPs. Commercial off-the-shelf (COTS) product was adapted in LFB system to save development time. In the future, Feedback software will be developed in continuously archiving operation version. Software to aid commissioning and for diagnostic purposes will be the highlight of the next step.

REFERENCES

[1] W. K. Lau et al: Study of Longitudinal Coupled-Bunch Instabilities in the SRRC Storage Ring, Proceedings of 1997 IEEE Particle Accelerator Conference, Vancouver, 1997.

[2] W. K. Lau, S. J. Lin, M. S. Yeh, L. H. Chang, T. T. Yang, K. T. Hsu, M. H. Wang, C. C. Kuo: Development Of A Digital Longitudinal Damper For The TLS Storage Ring, Proceedings of 1997 IEEE Particle Accelerator Conference, Vancouver, 1997.

[3] W. K. Lau, L. H. Chang, K. T. Hsu, C. H. Kuo, J. A. Li, M. S. J. Lin, T. T. Yang. M. S. Yeh: Progress of the TLS Longitudinal Feedback System and Associated Beam Longitudinal-Dynamics Studies, proceedings of 1999 IEEE Particle Accelerator Conference, New York, 1999.

[4] M. S. Yeh, K. T. Hsu, C. H. Kuo, W. K. Lau, J. F. Lee, S. J. Lin: High Speed Digital Processing Electronics for the TLS Longitudinal Feedback System, proceedings of 1999 IEEE Particle Accelerator Conference, New York, 1999.