# CONTROL SYSTEM OF THE SILICON MICROSTRIP LAYER FOR THE STAR EXPERIMENT

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*Abstract*

The Silicon Vertex Tracker (SVT) in the STAR experiment at RHIC makes use, in its outer layer, of silicon-strip detectors. This layer is a barrel of 320 double-sided detectors. The 768 strips of each detector's side are read out by 6 ALICE-128C analog front end chips. Those chips are remotely controlled, using a JTAG protocol. Another chip, the COSTAR, has been designed to perform *in situ* front end measurements (temperature, low and high voltage supplies, detector's bias currents). The Operator Interface is a Sun workstation, running EPICS. The Input Output Controller is a VME crate. The LAN is Ethernet, using the TCP/IP protocol.

## 1 INTRODUCTION

The STAR experiment (Solenoid Tracker At Rhic) will take place in the RHIC (Relativistic Heavy-Ion Collider) at BNL (Brookhaven National Laboratory USA) from the end of year 1999. The IReS (Institut de Recherche Subatomique at Strasbourg) in collaboration with the laboratory Subatech (Nantes) is responsible for the construction of a part of the experiment : the double-sided silicon strips detector (SSD). This detector is expected to measure the particle track position within a precision of about 30 micrometers. It is composed of 320 detection modules, which include the silicon detector and the front-end electronics (Alice 128C chips). It will be installed in the STAR experiment in the middle of the year 2000.
This document will describe the control system of the SSD layer.

## 2 ARCHITECTURE

### *2.1 Description of the system*

The system can be divided in two part :

- The slow control which purpose is to monitor the "slow" variables and parameters, essentially temperature and power supplies.
- The detector control which is involved in the initialization and calibration of the system, and the online analysis.

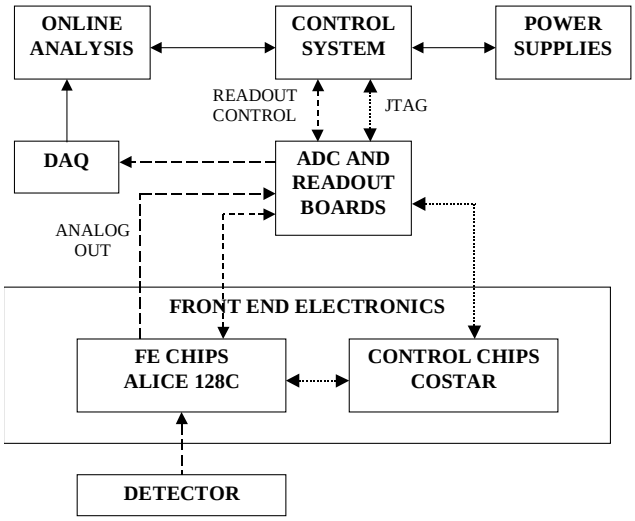


Figure 1: Block diagram of the system

### *2.2 Hardware*

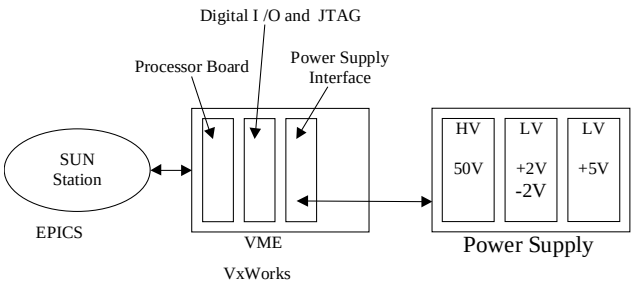


Figure 2: Hardware

A common design for the control of all parts of the STAR Detector has been decided by the STAR collaboration (Fig. 2). Basically, the control system is composed of a VME crate and a SUN workstation.
The VME crate is composed of a processor board running the VxWorks operating system and several interface boards.
The SUN workstation is the main user interface, running EPICS.

# 3 SLOW CONTROL

## *3.1 Monitored parameters*

The monitored parameters can be divided in two sets :

- The parameters measured by the COSTAR chip on each front end hybrid (there are 640 hybrids).
- The parameters measured by the power supply device. They are representative of one ladder (there are 20 ladders)

The table 1. shows the different slow control parameters.

| Parameters | Measured by | Number |
|---|---|---|
| Temperature | COSTAR | 640 |
| FEE voltage supplied | COSTAR | 1280 |
| Bias ring and guard ring currents | COSTAR | 1280 |
| Detector depletion voltage | Power supply | 20 |
| Detector leakage current | Power supply | 20 |
| FEE voltage | Power supply | 40 |
| FEE current | Power supply | 40 |
| Readout electronics voltage | Power supply | 20 |
| Readout electronics Current | Power supply | 20 |

Table 1. Monitored parameters

## *3.2 The COSTAR chip*

A general purpose chip has been designed to do *in situ* slow control measurements of JTAG operated detectors[1]. This chip has been designed by the LEPSI (Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux, Strasbourg, France), in collaboration with the IReS (Strasbourg, France). It is implanted on the hybrid of the STAR-SSD modules and is able to perform the following measurements:

- The temperature of the hybrid (measured by a probe integrated inside the chip). This information will be useful for controlling the effectiveness of the cooling system. The range is 0°C to 80°C, with a resolution of 0.5°C.
- The supplied voltages on the hybrid. These values can be compared with the supplied voltages in the ADC and readout boards (which are read through the sense lines of the power supplied devices) in order to detect any failure on the power lines of each hybrid (over current, short circuits, broken or resistive connection, etc.).
- The leakage currents of the bias and guard rings. This is carried out by measuring the voltage across a resistor inserted in the bias line of the hybrid. The bias and guard ring current values give us information about the status of the detector.

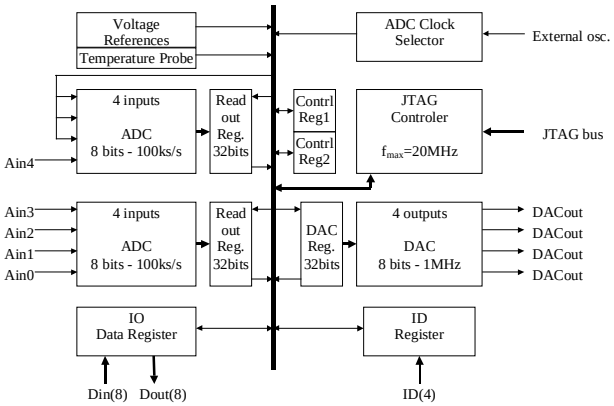


Figure 3: Block diagram of COSTAR

The architecture of the COSTAR is shown in Fig. 3. This chip is composed of ADCs, DACs and a digital I/O part that can be accessed through a JTAG bus. This allows several tasks to be performed which are useful for the Slow Control :

- Monitoring and control of analog parameters (through the ADCs and DACs). Up to five general purpose inputs and four general purpose outputs are available.
- Monitoring and control of digital parameters. An 8-bit input/output register is available for this purpose.

Amongst the eight ADC inputs available in the chip, three are dedicated to the conversion of internal temperature and supplied voltage values. The five others are external inputs, and two of them can be used for the measurement of bias and guard ring currents. In this application, the digital I/O and the DACs are not used.

In order to communicate with the slow control, the COSTAR uses the same JTAG bus as the Alice 128C chips. The connection to this bus does not require any additional components.

# 4 DETECTOR CONTROL

## *4.1 The Alice 128C chip*

The Alice 128C chip has been designed by the LEPSI in collaboration with the IReS [2].
It is a 128 channels low power chip which contains all parts of the front end electronics : pre-amplifier, shaper, multiplexer, internal pulse generator, etc.
All this parts can be remotely configured via a JTAG bus. This allows us to remotely control such parameters as the shaping time, gain, internal pulse generator level, etc.
The table 2. shows the registers controlled by the JTAG bus in the Alice 128C.

| Parameter | Size (bits) |
|---|---|
| Bias register (analog chain parameters) | 56 |
| Pulse level | 8 |
| Pulse generator selected channels | 128 |
| Output multiplexer | 258 |
| Output buffer power | 1 |
| Readout Token Enable | 1 |

Table 2. Alice 128C registers

### *4.2 Configuration setting*

Once the run configuration has been decided, it has to set up the detector in the appropriate state. This involves communication with DAQ, slow control, and any software/hardware required to operate the detector. A database, with all the configuration parameters stored in it, is read and the parameters initialized in the target system.

### *4.3 Online analysis*

During a run, some kind of raw data analysis has to be carried out, to check whether the response of the detector is coherent. This online analysis should be made on a fraction of the events, and the results should be displayed with histograms on an online monitor screen.

## 5 CONCLUSION

The hardware used in this control system is now well defined and has been tested during the characterization of the first prototype detection module (at CERN SPS and PS, September-October 1999).
Most of the job to be done for now concerns the software part, i.e. :

- EPICS drivers and user interface
- Online analysis
- Configuration database

## 6 REFERENCES


[1] J.D. Berst, C. Colledani, “COSTAR”, Costar Note V0.1-Lepsi9904 – Laboratoire d’Electronique et de Physique des Système Instrumentaux , April 99.

[2] J.R. Lutz and al., “Electrical characterization of ALICE128C: a low power CMOS ASIC for the readout of silicon strip detectors”, 4th Workshop on Electronics for LHC Experiments, Rome (Italy), September 1998.