THE CONTROL SYSTEM OF THE MAIN MAGNET POWER SUPPLY IN NSRL

Weimin Li, Songqiang Liu, Jingyi Li, Gongfa Liu, Shouming Hu,
National Synchrotron Radiation Lab, Anhui, Hefei 230029, China

Abstract

The control system of main magnet power supplies (PS) in NSRL electron storage ring is built upon the Experimental Physics and Industrial Control System (EPICS). Because PCs have become more and more popular in accelerator control, We use Industrial PC (IPC) as the low-level controller, i.e. front-end device controller (FDC). A total of 12 FDCs control a group of 12 PSs respectively. PSs are star connected to an Input / Output controller (IOC) via RS422. The IOC is an IPC on which vxWorks runs to meet the demand of EPICS. A SUN workstation is used as an OPI (Operator Interface) as well as an EPICS server.

1 INTRODUCTION

The electron storage ring of NSRL is a dedicated synchrotron light source in which the electrons circulate at the energy of 800Mev. It is a four-period machine. In each period, there are 3 dipole magnets, 8 quadruple magnets and 3 sextuple magnets. We call these magnets main magnets. All of the dipole magnets share one power supply. There are 8 power supplies for quadruple magnets and 3 power supplies for sextuple magnets. The magnets of each period share the same group of power supplies. Before the control system upgrade, all main magnet power supplies were controlled by MULTIBUS-I based controllers, which are star connected to higher level computer via RS422. An 80486 PC was used both for the high-level controller and operator interface [1]. This system was upgraded starting in 1997. It is now an EPICS-based control system. Because PCs are becoming more and more popular in control systems, we now use industrial PCs as the low-level device controllers. We also use an IPC as the IOC. All device controllers are star-connected to the IOC via optically-coupled RS422. A Sun workstation is used as man-machine OPI.

2 OWERVIEW OF THE CONTROL SYSTEM

The main magnet power supply control system was built upon EPICS. It is a subsystem of the NSRL accelerator control system. Fig.1 shows the structure of the main magnet power supply control system.

We use a SUN workstation as the OPI. There are several MEDM screens for man-machine interface. We also use a number of TCL/TK scripts to do complicated control. Database definitions and EPICS software are also reside on this workstation. An IPC with a Pentium II 350 CPU is used the IOC and communicates with FDCs via optically-coupled RS422. In order for the IOC to communicate with a group of 12 FDCs, we added two multi-port RS422 cards to the IPC. We also developed a driver for the multi-port cards, and finally integrated the ports as tty devices. In order to provide high-speed communication between OPIs and IOCs, we use 100M Ethernet at the network level. An Intel Pro/100+ Ethernet card was added to the IOC crate to provide an interface between the IOC and the network. The FDC is also PC-based hardware, which will be described in detail in the following section.

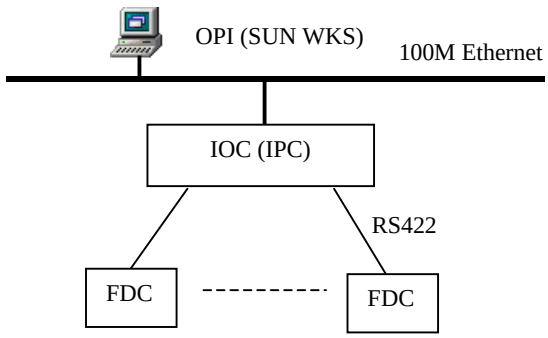

Fig 1 Structure of main PS control system

3 FRONT-END DEVICE CONTROLLER

3.1 Hardware description

We used PC-based hardware as the front-end device controller. Fig 2 shows the hardware skeleton of FDC.

- An Optically-coupled RS422 module is used to provide a way to communicate with the IOC. The speed can be as high as 115.2kbps [2].
- A 16 bits DAC module is used to control the set-point value of each P.S.
- A 16 bits ADC module is used to get high resolution values from DCCT.
- A 4 Chan. Relay/8 chan. digital input module is used to control the P.S. and monitor P.S. status.
- A Timer/Counter is used to control the ramp procedure.

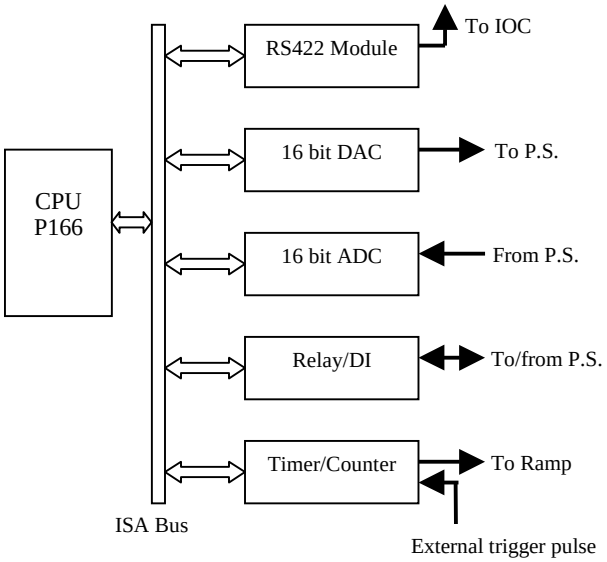

Fig 1. Front-end Device Control of Main P.S.

3.2 Software

The software of FDC is based upon vxWorks real-time operation system. The functional diagram is showed in fig 2.

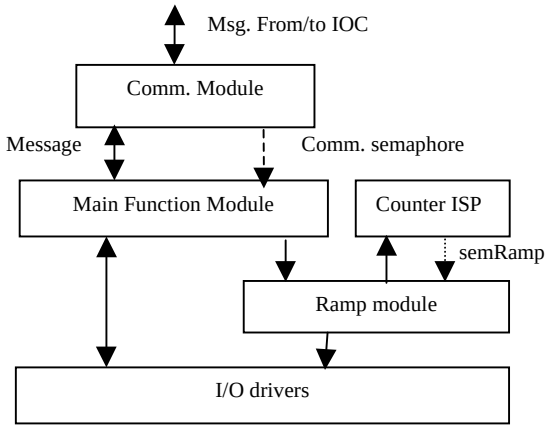

Fig 2. FDC software functional diagram

- Communication module. The main function of the communication module is to accept a message from upper level controller (IOC) and then check if the message is accurate. If so, a semaphore is produced, which will be taken by the main function module. If the command in the message is a kind of read command, the communication module also has the obligation to send back the response message.
- Main function module. When a semaphore is given, this module takes the semaphore and reads the message accepted from the IOC by the communication module. After that, the main function module parses the message. If the command from the message is a kind of write command, the module calls the corresponding driver to set corresponding channel to the value from the message. If the command is a kind of read one, the module calls the corresponding driver to read the corresponding channel and then send back the response message via the communication module.
- Ramping module. When it gets a ramp start command, which is a kind of write command, the main function module calls a channel driver dedicated to the ramping module, which will prepare to spawn a ramp module. The newly-spawned ramp module will prepare for the ramp procedure first. Then it waits for a semaphore. The semaphore is given by counter interrupt service procedure (ISP) to let the ramp module to go up/down a step.
- Counter ISP. When the counter value, which is set by the ramp module on the fly, comes down to zero, an interrupt occurs, and the counter ISP is then called to give a ramp semaphore to cause the ramp module to go up/down a step. The counter is triggered by an external time pulse.
- There are a number of I/O and/or virtual channel drivers to provide a way to access corresponding hardware/software channels.

4 SUMMARY

Because the IPC applies industrial standard, the IOC is reliable enough to control the main PS. A Pentium II 350 CPU makes the IOC much faster than 680xx CPUs [3]. 100M Ethernet can make the CA process much faster.

For the FDC, we took a number of measures to avoid EMI. We also made great efforts to get high- resolution ADC values and high stability DAC outputs.

We have tested the system in simulation mode, and the results have shown that this system meets main PS control demands.

ACKNOWLEDGEMENTS

Special thanks to Dr. Wu at FEL lab, Duke university. Also thanks to all the people who have given us so much help at EPICS tech-talk.

REFERENCES

[1] Weimin Li et al, ICALEPS' 97 Beijing, China, 1997, p19.
[2] Gongfa Liu, "Application of PCs in NSRL Control system", this proceeding.
[3] J.O.Hill, ICALEPCS, IHEP, Beijing, China, 1997, p.169.